REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with N.O.R. 5962-R057-93.	92-12-29	M. A. FRYE
B	Drawing updated to reflect current requirements. - ro	02-03-07	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B			
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY
DAN WONNELL

CHECKED BY
SANDRA ROONEY

APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
92-07-15

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, DIGITAL TO ANALOG CONVERTER, 12 BIT, HIGH SPEED,

MONOLITHIC SILICON

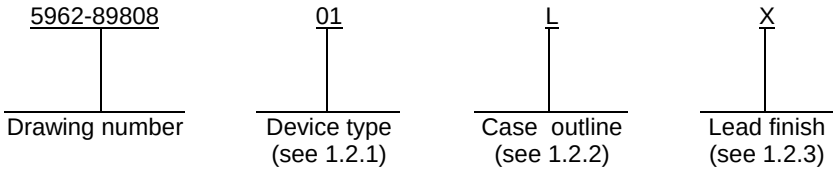
SIZE	CAGE CODE	
A	**67268**	**5962-89808**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD568SQ	12-bit high speed D/A converter
02	AD568SE	12-bit high speed D/A converter

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{CC} to reference common range ..... 0 V dc to +18 V dc
V_{EE} to reference common range ..... 0 V dc to -18 V dc
Reference common to ladder common range ..... +100 mV to -10 V dc
Analog common to ladder common ..... ±100 mV
Threshold common to ladder common ..... ±500 mV
10 V span resistor to ladder common ..... ±12 V
Bipolar offset to ladder common ..... ±5 V
I_{OUT} to ladder common ..... -5 V dc to threshold control
Digital inputs to threshold common range ..... -500 mV to +7.0 V dc
Voltage across span resistor ..... 12 V dc
Threshold control to threshold common range ..... -0.7 V dc to +1.4 V dc
Logic threshold control input current ..... 5 mA
Power dissipation (P_D):
  Cases J and L ..... 1000 mW
  Case 3 ..... 600 mW
Storage temperature range ..... -65°C to +150°C
Junction temperature (T_J) ..... 200°C

1.3 Absolute maximum ratings.

Thermal resistance junction-to-case (θ_{JC}):
Cases J and L ..... 25°C/W
Case 3 ..... 42°C/W
Thermal resistance junction-to-ambient (θ_{JA}):
Cases J and L ..... 75°C/W
Case 3 ..... 125°C/W

1.4 Recommended operating conditions.

V_{CC} to reference common range ..... +13.5 V dc to +16.5 V dc
V_{EE} to reference common range ..... -13.5 V dc to -16.5 V dc
Ambient operating temperature range (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Relative accuracy	RA	I_{OUT} mode	1	All	-0.5	+0.5	LSB
			2,3	01	-0.75	+0.75	
				02	-1	+1	
Differential nonlinearity	DNL	I_{OUT} mode	1,2,3	All	-1	+1	LSB
Gain error	A_E	All bits on, I_{OUT} mode	1	All	-1	+1	% of FSR
Gain drift temperature coefficient	TCA_E	All bits on, V_{OUT} mode	2,3	01	-50	+50	ppm of FSR/°C
				02	-60	+60	
		All bits on, I_{OUT} mode		All	-150	+150	
Unipolar offset	U_{OS}	All bits off, I_{OUT} mode	1	All	-0.2	+0.2	% of FSR
Unipolar offset temperature coefficient	TCU_{OS}	All bits off, V_{OUT} mode	2,3	All	-5	+5	ppm of FSR/°C
Bipolar offset	B_{POS}	I_{OUT} mode, all bits off bipolar	1	All	-1.0	+1.0	% of FSR
Bipolar offset temperature coefficient	TCB_{POS}	V_{OUT} mode, all bits off bipolar	2,3	01	-30	+30	ppm of FSR/°C
				02	-40	+40	
Bipolar zero	B_{PZE}	I_{OUT} mode, MSB on, all other bits off bipolar	1	All	-0.2	+0.2	% of FSR
Bipolar zero temperature coefficient	TCB_{PZE}	V_{OUT} mode, MSB on, all other bits off bipolar	2,3	All	-15	+15	ppm of FSR/°C
High input voltage	V_{IH}		1,2,3	All	2.0	7.0	V
Low input voltage	V_{IL}		1,2,3	All	0.0	0.8	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
High input current	I_{IH}	V_{IH} = 7 V	1,2,3	All	-10.0	+10.0	µA
Low input current	I_{IL}	V_{IL} = 0.0 V	1	All	-100	-0.5	µA
			2,3		-200	-0.5	
Output current	I_O	Unipolar, all bits on	1	All	10.137	10.343	mA
			2,3		9.985	10.50	
		Bipolar, all bits on	1		5.017	5.223	
			2,3		4.942	5.300	
Output voltage	V_O	Unipolar, all bits on	1	All	1.014	1.034	V
			2,3		1.008	1.040	
		Bipolar, all bits on	1		0.507	0.517	
			2,3		0.504	0.520	
Compliance voltage	V_C	2/	1,2,3	All	-2	+1.2	V
Output resistance exclusive of R_L	R_{OE}	2/	1,2,3	All	160	240	Ω
Output resistance inclusive of R_L	R_{OI}	2/	1,2,3	All	99	101	Ω
Settling time	t_{SL}	Current to ±0.025 % of FSR 2/	9	All		120	ns
			10,11			165	
		Current to ±0.1 % of FSR 2/	9			125	
			10,11			130	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{EE} = -15 V unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Rise time	t_R	From 10 % to 90 %, 2/ V_{OUT} mode	9,10,11	All		20	ns
Fall time	t_F	From 90 % to 10 %, 2/ V_{OUT} mode	9,10,11	All		20	ns
Power supply current	I_{CC}	V_{CC} = 16.5 V, V_{EE} = -16.5 V, V_{OUT} = 5 V	1,2,3	All		32	mA
	I_{EE}	V_{CC} = 16.5 V, V_{EE} = -16.5 V, V_{OUT} = 5 V			-8		
Power supply rejection ratio	+PSRR	13.5 V $\le V_{CC} \le$ 16.5 V,	1	All		0.05	% of FSR/V
		V_{EE} = -15 V	2,3			0.06	
	-PSRR	-13.5 V $\le V_{EE} \le$ -16.5 V,	1			0.05	
		V_{CC} = 15 V	2,3			0.06	

1/ The algebraic convention whereby the most negative value is minimum and the most positive a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

2/ If not tested, shall be guaranteed to the limits specified in table I herein.

Device types	01	02
Case outlines	J and L	3
Terminal number	Terminal symbol	
1	BIT 1 (MSB)	NC
2	BIT 2	BIT 1 (MSB)
3	BIT 3	BIT 2
4	BIT 4	BIT 3
5	BIT 5	BIT 4
6	BIT 6	BIT 5
7	BIT 7	BIT 6
8	BIT 8	NC
9	BIT 9	BIT 7
10	BIT 10	BIT 8
11	BIT 11	BIT 9
12	BIT 12 (LSB)	BIT 10
13	THRESHOLD CONTROL (V_{TH})	BIT 11
14	THRESHOLD COMMON (THCOM)	BIT 12 (LSB)
15	10 V SPAN RESISTOR	NC
16	10 V SPAN RESISTOR	THRESHOLD CONTROL (V_{TH})
17	LADDER COMMON (LCOM)	THRESHOLD COMMON (THCOM)
18	ANALOG COMMON (ACOM)	10 V SPAN RESISTOR
19	LOAD RESISTOR (RL)	10 V SPAN RESISTOR
20	I_{OUT}	LADDER COMMON (LCOM)
21	BIPOLAR OFFSET (I_{BPO})	ANALOG COMMON (ACOM)
22	V_{EE}	NC
23	REFERENCE COMMON (REFCOM)	LOAD RESISTOR (RL)
24	V_{CC}	I_{OUT}
25	---	BIPOLAR OFFSET (I_{BPO})
26	---	V_{EE}
27	---	REFERENCE COMMON (REFCOM)
28	---	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

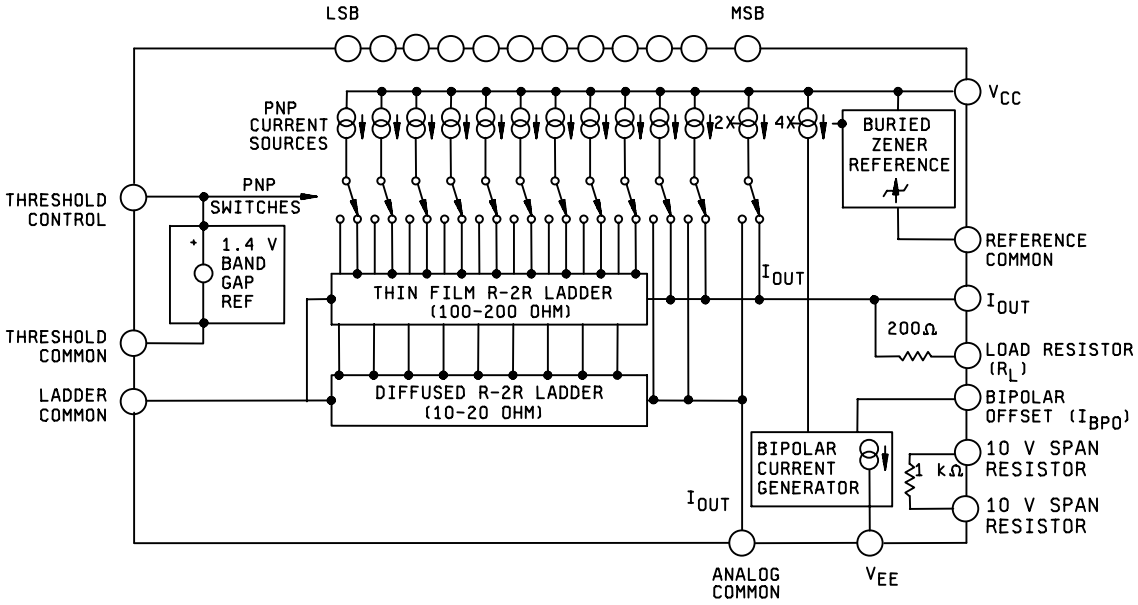


FIGURE 2. Functional block diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3
Group A test requirements (method 5005)	1,2,3,9**,10**,11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 9, 10, and 11, if not tested, shall be guaranteed.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-03-07

Approved sources of supply for SMD 5962-89808 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8980801JA	3/	AD568SQ/883B
5962-8980801LA	24355	AD568SQ/883B
5962-89808023A	3/	AD568SE/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 804 Woburn Street Wilmington, MA 01887-3462